

A DC to 10-GHz 6-b RF MEMS Time Delay Circuit

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Abstract—A 6-b radio frequency (RF) microelectromechanical system (MEMS) time delay circuit operating from dc to 10 GHz with 393.75-ps total time delay is presented. The circuit is fabricated on 250- μm -thick alumina and uses metal contacting RF MEMS switches to realize series-shunt SP4T switching networks. The circuit demonstrates $1.8 + / - 0.6$ dB of loss at 10 GHz and has linear phase response across the entire band with accuracy of better than a least significant bit for most states.

Index Terms—Delay circuits, microelectromechanical (MEMS) devices, microwave phase shifters, switches.

I. INTRODUCTION

LOW loss time delay circuits with a flat delay response across the entire band are essential for realizing large passive antenna arrays [1]. Broadband operation precludes taking advantage of the 360° phase reentrance of the radio frequency (RF) signal, requiring time delays of several wavelengths to maintain proper beam steering for a large array. To maintain steering resolution, this additional delay can only be obtained by increasing the number of bits of the time delay circuit.

Radio frequency microelectromechanical systems (RF MEMS) provide the best combination of high linearity, flat delay, low loss, and small size for these applications [2]. Numerous RF MEMS time delay circuits and phase shifters with up to 4 b of time delay have been reported in the literature, using switched line [3]–[5], distributed transmission line [6], [7], reflect-line [8], [9], and quasilumped element [10] approaches. However, these circuits have been limited to 4 b of delay and time delays of 100 ps or less, corresponding to 360° maximum phase shift with 22.5° resolution at 10 GHz. While each time delay approach has specific benefits and drawbacks, the switched line topology is the only practical topology for meeting the long delay and broadband performance required for these antenna arrays.

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A 6-b, multiwavelength time delay circuit presents additional challenges when compared to previously reported 4-b, single-wavelength delay circuits. These specific challenges include minimizing resonances due to the multiwavelength delay lines, maintaining return loss for an all-passive 6-b cascade, and achieving large time delays within a moderate die size while minimizing coupling between lines.

In this work, we have realized a 6-b time delay circuit with a most significant bit of 200 ps and a total delay of 393.75 ps. This circuit produces a maximum delay of four wavelengths at the highest operating frequency of 10 GHz while maintaining a tuning resolution of 22.5° at 10 GHz. To our knowledge, this is the first demonstration of an RF MEMS time delay circuit with greater than 4 b of delay and a maximum delay greater than 100 ps at these frequencies.

II. TIME DELAY CIRCUIT DESIGN

The circuit was designed as a cascade of 2-b time delay circuits [3], which is a compromise between the number of series switches in a delay path and the complexity of the multipole switching network used to realize the circuit. Each 2-b circuit uses two single pole four throw (SP4T) switching networks to select between the reference line and the three available delay lines.

The design of the SP4T switch has a direct impact on the group delay flatness, return loss, and insertion loss of the circuit. In addition to the group delay variation caused by the impedance matching network at the switch, group delay variation may occur with insufficient switch isolation due to the changing reactance of the off-state paths coupled through the open switches. Additionally, the off-paths will resonate near multiples of their half-wavelength frequency [11]. This resonance will couple in through the switch and cause a resonance in the insertion loss, return loss, and group delay of the circuit. While the changing off-path reactance may be addressed by increasing switch isolation, the off-path resonances will couple to the through path for any noninfinite switch isolation. These off-path resonances were not a significant problem in previously reported time delay circuit designs because the total delays were only one or two wavelengths long at the highest frequency of interest.

A series-shunt SP4T switch was developed to obtain the required performance for the time delay circuit. The input matching procedure and junction design was based on the procedure used by Tan [3], while the addition of the shunt switch improved the isolation of the SP4T switch from 33 dB to 38 dB at 10 GHz. More importantly, the shunt switch damps

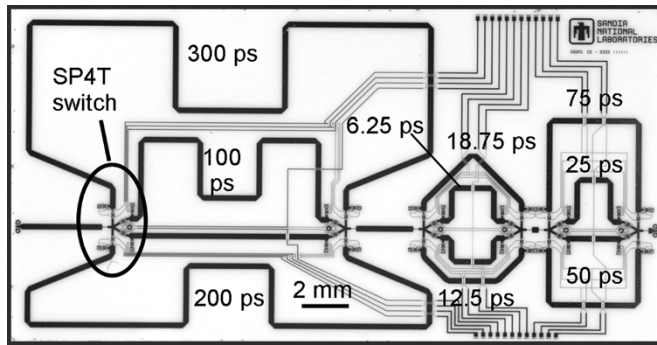


Fig. 1. Optical micrograph of the RF MEMS 6-b time delay circuit. The die size is 27 mm \times 14 mm.

the off-path resonance by grounding the ends of the transmission line, preventing excitation of the off-state line through the capacitance of the open switch. From dc to 10 GHz, the insertion loss of the switch is lower than 0.2 dB and return loss better than 20 dB.

The switching networks and delay lines were simulated using both circuit level simulation [12] and electromagnetic simulation [13]. Electromagnetic simulation was used to simulate more complex structures such as the junction network in the SP4T switch and transmission line corners. Because broadside coupling will also generate resonances in the circuit, coupling between lines was controlled by minimizing long lengths of adjacent parallel lines.

III. RF MEMS SWITCHING TECHNOLOGY

The circuits were fabricated on 76-mm-diameter, 250- μ m-thick alumina with CuW-filled via holes and a 25-nm final polish. This substrate is the best substrate for these microstrip circuits when metal loss, radiation losses, dispersion, and ease of circuit layout are considered. The RF MEMS switching technology used to realize this circuit is similar to that described earlier [14]. The microstrip transmission lines are 2- μ m-thick gold while the switch body is 6.5- μ m-thick gold electroplated on top of a photoresist sacrificial layer, which is removed by wet processing. The switch utilizes Au–Au contacts and demonstrates insertion loss less than 0.1 dB and isolation better than 30 dB at 10 GHz. A 1-k Ω /sq TaN resistor layer is used for bias routing without significantly impacting the RF performance of the circuit. Folded springs minimize the impact of residual stress, thermal stresses, and stress gradients, allowing operation from -25°C to $+125^\circ\text{C}$.

The 6-b time delay circuit, shown in Fig. 1, employs 48 RF MEMS switches and occupies a die area of 27 mm \times 14 mm. Switch yields were approximately 96%, resulting in circuit yields of about 15%. Efforts to improve the reproducibility, yield, and reliability of the RF MEMS switch process are underway and are expected to improve the manufacturability of this circuit.

IV. TIME DELAY CIRCUIT RESULTS

The unpackaged time delay circuits were tested from 100 MHz to 10 GHz using an HP 8510C vector network analyzer in conjunction with a Cascade Summit on-wafer probe station. The system was calibrated at the probe tips using the

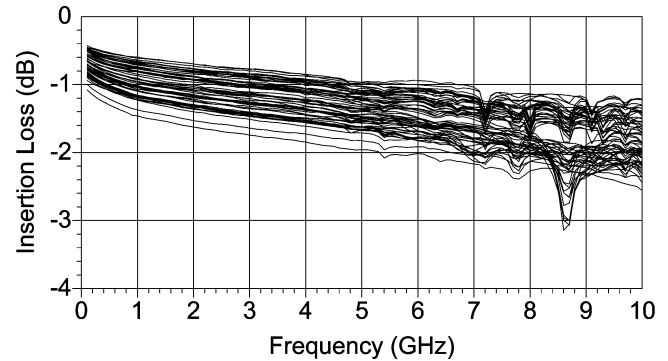


Fig. 2. Measured insertion loss of the 6-b RF MEMS time delay circuit.

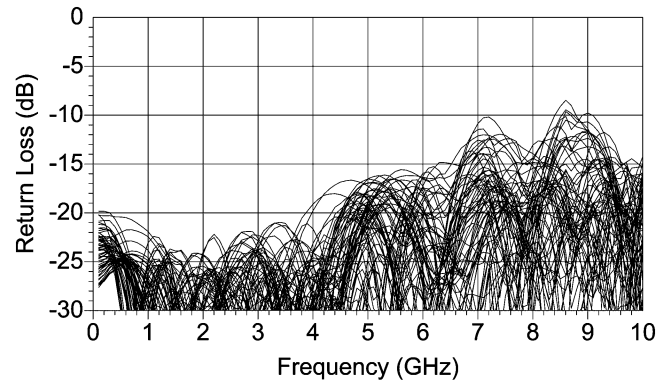


Fig. 3. Measured return loss of the 6-b time delay circuit.

LRRM method. A dc power supply and switching matrix was used to actuate the switches.

The insertion loss for all 64 delay states of the circuit is shown in Fig. 2. The insertion loss at 10 GHz ranges from 1.2 dB to 2.4 dB, with an average of 1.8 dB. The insertion loss is as high as 3.1 dB between 7 and 9 GHz due to resonances from broadside coupling between the closely spaced lines in the center small time delay circuit. Broadside coupling was reduced but not eliminated by limiting parallel lengths of lines, but the short differences in delay length for the smallest circuit forced close routing of lines. This problem can be addressed by designing additional reference length into all of the lines in the small circuit.

This measured insertion loss is similar to the expected insertion loss of 2.15 ± 0.35 dB calculated by assuming 0.2 dB of loss per SP4T switching network (1.2 dB total), a transmission line loss of 0.15 dB/cm at 10 GHz for a reference length of 1.9 cm (0.3 dB total) and a maximum delay length of 6.5 cm (1.0 dB total), and a mismatch loss of 0.3 dB.

The return loss of all 64 delay states of the circuit is shown in Fig. 3. The return loss is better than 15 dB through 6 GHz and better than 10 dB across the entire band with the exception of the previously discussed resonance at 9 GHz. The return loss is difficult to optimize for this long cascade of passive networks, but is much better than the 5-dB worst case return loss predicted by cascade theory because the reflected signals combine out of phase across most of the band.

The differential phase response of the circuit is shown in Fig. 4, showing the linear phase delay required for broadband antenna steering. The majority of the individual phase traces are well-spaced, with no overlapping or crossing traces. The only

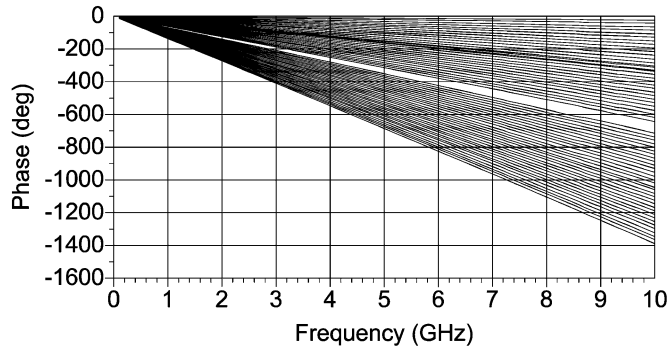


Fig. 4. Measured differential phase response of the time delay circuit.

exception is due to the 100-ps-delay line, which is slightly too short, shifting a set of 16 lines up by 13 ps and causing overlap with the upper set of lines and a gap between the 193.75-ps state (binary value 011 111) and the 200-ps state (100 000). The 300-ps-delay line is also 6 ps. too short, narrowing the gap between the 293.75-ps state (101 111) and the 300-ps state (110 000). All of the other delay errors are less than 2.2 ps, which is less than half a least significant bit. The delay errors were determined by calculating a phase error at 10 GHz and converting to an equivalent phase delay error in ps. The error was calculated in this manner rather than using group delay to eliminate uncertainty due to noise in the group delay measurement. Delay errors can be corrected by adjusting the delay lines on future design iterations.

Microstrip dispersion causes a delay variation of 0.6% from 0.1 to 10 GHz, increasing the delay by less than 3 ps from the lowest measured frequency to the highest frequency in the longest delay state. This error is less than half of a least significant bit and varies slowly across the band, so it should not degrade the steering performance of a broadband antenna array.

V. FUTURE WORK

While this time delay circuit demonstrates insertion loss, return loss, and phase delay performance suitable for phased array antenna applications, several problems must be addressed prior to fielding in a system. Future tasks include addressing the delay errors and resonances, improving the yield and reliability of the MEMS technology, and packaging the time delay circuit. Additionally, exploring methods to reduce the die area of the circuit will be essential to inserting it into an antenna array tile, suggesting the need for three-dimensional integration or quasilumped delay lines.

VI. CONCLUSION

The first 6-b RF MEMS time delay circuit has been demonstrated for broadband antenna array applications operating from dc to 10 GHz. The time delay circuit delivers four wavelengths of delay at the highest frequency while maintaining 4 b per wavelength of delay resolution for fine antenna steering. Low loss substrates and materials have allowed an extremely low insertion loss of 1.8 ± 0.6 dB at 10 GHz and linear phase with only 0.6% dispersion in phase delay between 0.1 and 10 GHz. This circuit is the first 6-b RF MEMS time delay circuit and demonstrates the potential of RF MEMS for high-order, multiwavelength time delay networks for phased array antenna applications.

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